CLAIMS

We Claim:

1. In an integrated circuit package, a lead frame comprising:

a die attach platform;

a plurality of elongated leads which are electrically isolated from said die attach platform; and

a first bus bar which is electrically isolated from said die attach platform and said plurality of elongated leads.

2. The package of Claim 1 wherein:

said lead frame further comprises a second bus bar which is electrically isolated from said die attach platform, said plurality of elongated leads, and said first bus bar;

said die attach pad is positioned between said first and second bus bars; and

said plurality of elongated leads extend radially away from said first and second bus bars and said die attach platform.

3. The package of Claim 2 further comprising an integrated circuit chip mounted on said die attach platform, said integrated circuit chip having a plurality of power I/O pads, a plurality of ground I/O pads, and a plurality of signal I/O pads, wherein:

each of said plurality of signal I/O pads is electrically connected with a selected one of said plurality of leads;

said plurality of power I/O pads are electrically connected to said first bus bar; and

said plurality of ground I/O pads are electrically connected to said second bus bar.

4. The package of Claim 2 further comprising an integrated circuit chip mounted on said die attach platform, said integrated circuit chip having a plurality of power I/O pads, a plurality of ground I/O pads, and a plurality of signal I/O pads, wherein:

each of said plurality of signal I/O pads is electrically connected with a selected one of said plurality of leads;

said plurality of power I/O pads are electrically connected to said first bus bar or said second bus bar; and

said plurality of ground I/O pads are electrically connected to said die attach platform.

5. The package of Claim 3, wherein said lead frame is substantially co-planar, having opposing first and second surfaces, and wherein said integrated circuit chip is attached on the first surface of said die attach platform, further comprising:

a mask layer formed on the second surface of said lead frame, said mask layer defining a plurality of openings exposing selected portions of said plurality of leads; and

a plurality of solder balls, each of said plurality of solder balls being connected to one of said plurality of leads through one of said plurality of openings.

6. The package of Claim 5 wherein said mask layer comprises a solder mask.

7. The package of Claim 6 wherein said mask layer comprises a plated layer, the material of said plating layer being resistant to solder flow.

8. The package of Claim 3 wherein:

said first bus bar is electrically connected to one of said plurality of leads that is designated to be electrically connected to the external power supply of said integrated circuit chip;

said second bus bar is electrically connected to the one of said plurality of leads that is designated to be electrically connected to ground potential; and

said lead frame and said integrated circuit chip are encapsulated in a protective casing.

9. In an integrated circuit (IC) package including a lead frame and an IC chip, wherein said IC chip includes a plurality of I/O pads for signal communications and a portion of said plurality of said I/O pads require a common signal, a method for increasing the chip pinout of said IC chip without increasing the module pinout of said IC package comprising the steps of:

creating a bus bar in said lead frame; and

electrically connecting said portion of said plurality of said I/O pads to said bus bar.

10. In a lead frame ball grid array (BGA) package, a lead frame comprising:

a die attach platform;

a plurality of elongated leads which are electrically isolated from said die attach platform; and

a plurality of circular attachment pads, wherein each of said plurality of elongated leads is connected to a unique one of said plurality of circular attachment pads, each of said plurality of circular attachment pads being sized to provide a desired attachment area for a specified solder ball and being

located to provide a desired electrical interconnection between said BGA package and a host PCB.

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